IN THE SPECIFICATION

Please amend the specification as follows:

Please replace the paragraph beginning at page 6, line 11, with the following rewritten paragraph as follows:

-- In order to achieve the above described object, in accordance with an aspect of the present invention, an advanced or speculative read request is issued to a controller of the cache data portion before conducting the cache hit check. Thus, data supplied from the cache is read in advance and held in the controller. In the case where a cache hit has occurred, the read request based on the cache hit check is issued to the controller to read the data subjected to advanced speculative readout is read out. --

Please replace the paragraph beginning at page 11, line 26 through page 12, with the following rewritten paragraph as follows:

-- By referring to the cache tag section 5, the coherent controller 20 determines whether the received memory access request hits the cache. However, if, in the case of a read request, a data is read out from the cache data section cache 7 via the cache data controller based on a result of the cache hit decision is obtained, the access latency becomes large. Then, before conducting a cache hit decision by referring to the cache tag section 5, the coherent controller 20 issues a request for conducting advanced or speculative readout to the cache data controller 6 (when the readout request is received from the processor bus). The speculative (SP) readout request may be formatted to include an address area, a read/write ID area and a SP

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bit area indicating whether the request is speculative. Otherwise the request may be formatted by only an entry address, if it is speculative. Thus, the coherent controller 20 reads out data which should be read out when a hit has occurred, from the cache data section 7 into the cache data controller 6 in advance. When a hit has occurred, the coherent controller 20 uses this data read in advance. --

Please replace the paragraph beginning at page 23, line 4, with the following rewritten paragraph as follows:

-- Fig. 11 is a processing flow of the request controller 400 included in the cache data controller 6. Fig. 11 is different from Fig. 9 in that steps 900 and 901 have been added. The steps 900 and 901 are a processing flow conducted in the case where a speculative read ~~cancellation~~ discarding request has been accepted from the coherent controller 20. In other words, upon receiving a speculative read data discarding request from the coherent controller 20 (step 900), the request controller 400 invalidates an entry in the speculative read request buffer 401 in which a cache entry number of a speculative read request corresponding to the pertinent speculative read data cancellation request has been registered (step 901). As a result, effective use of the speculative read request buffer 401 and the speculative read data buffers 403 to 406 becomes possible. If each of the buffers 401 and 403 to 406 is formed with a margin of a certain degree in the number of entries, it becomes possible to eliminate the full state and it also becomes possible to make the full control itself of the steps 703 and 704 unnecessary. --